

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 1, LINE 19 ENDING ON PAGE 2, LINE 5**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

One way in which circuit resistance is decreased is by creating low-resistance, ohmic contacts at the device level. Ohmic contacts exhibit nearly linear current-voltage characteristics in both directions of current flow. Various factors affect the type of contact which is maintained. Increasing dopant concentration in the semiconductor contact area decreases contact resistance, up to the solubility of the dopant at the temperature at which it is introduced. Unclean semiconductor surfaces (i.e., those which contain a native oxide film) increase contact resistance. Native oxides are a problem due to silicon's rapid oxidation rate when exposed to an oxygen ambient. The most widely used method for removal of such oxides is by dipping the wafer in a hydrofluoric acid solution. However, this does not perfect cleaning of the semiconductor substrate because some native oxide forms between the time of the hydrofluoric acid dip and the deposition of metal contacts. Sputter etching has been used in an attempt to alleviate this imperfection, but it falls short because more oxide is introduced onto the semiconductor substrate than is removed.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 3, LINE 16 ENDING ON PAGE 3, LINE 22**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

A primary method for depositing films by PVD is sputtering. Sputtering is a method by which atoms on a target are displaced to a desired surface, where they form a thin film. One possible solution to the problem of over consumption of silicon in shallow junctions is to use a PVD process to deposit a metal/silicon alloy, like titanium silicide. When the deposited material is an alloy, the target is generally a composite target consisting of two or more materials mechanically arranged in a selected ratio, to yield a film of the desired alloy composition.

09/567,574

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 4, LINE 12 ENDING ON PAGE 4, LINE 20**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

A recess feature is defined by an upper and a lower surface. An alloy is deposited in a recess feature of a semiconductor substrate by sputtering an alloy or composite target onto the semiconductor substrate to form a layer of deposited material on the upper surface. After a period of time, a negative bias voltage is applied to the substrate, initiating a resputtering scheme, which operates simultaneously with the sputtering step. The layer of deposited material is resputtered, to redeposit the layer of deposited material onto the lower surface as a first layer of resputtered material having a different stoichiometry than that of the deposited material. The resulting recess has improved bottom step coverage, which results in improved ohmic contacts.

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**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 15 ENDING ON PAGE 6, LINE 25**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

In one embodiment of the invention, a collimated PVD setup is used to obtain a low grazing angle during resputtering. In a second embodiment of the invention, a long-throw process is used to obtain a low, grazing angle during resputtering. A long-throw process utilizes a non-collimated PVD apparatus. During a long-throw process, spacing between a target and substrate is so large that only a portion of target material, having a small trajectory angle, with respect to the normal direction of the target, can reach the bottom of a contact hole. Note that in the case of resputtering material overhang, the normal direction of the target (material overhang) is measured, extending radially into the contact hole, in the plane of the substrate. The resulting material deposition rate and bottom step coverage are improved using this embodiment, due to the low energy and low angle mechanisms described previously.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 26 ENDING ON PAGE 7, LINE 5**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

In a further embodiment of the invention, a sputtering chamber ambient atmosphere comprises argon and a nitrogen concentration of between approximately 0.1 to 3.0 percent by volume. Furthermore, in yet another embodiment of the invention, the resputtering step is followed by resputtering of at least one layer of material with a different stoichiometry than that of the first resputtered material layer, to form a "graded" stoichiometry of material deposited in the contact hole. Using a nitrogen ambient increases the ion-to-neutral ratio, which increases the resputtering rate. Therefore, the resulting material deposition rate and bottom step coverage are improved using this embodiment.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 7, LINE 17 ENDING ON PAGE 7, LINE 18**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

[Figure 3 is] Figures 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

FIG. 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 8, LINE 1 ENDING ON PAGE 8, LINE 4**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

Existing equipment, such as a Varian M2000 PVD apparatus, is utilized to accomplish better bottom step coverage. The invention does not require purchasing a new deposition system and training employees on how to use it, saving cost and time in fabricating contacts for semiconductor devices.

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**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 9, LINE 26 ENDING ON PAGE 10, LINE 7**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

A process window starts by introducing an inert gas, such as argon, from a gas inlet (not shown here), through region 222 and into the space between the target 236 and substrate 200 to form a plasma 240, and allowing it to stabilize (approximately 5 to 10 seconds), as shown in Figure 2. Placing the gas under low, sub-atmospheric pressure creates the plasma (i.e., a mixture of positively charged gas ions and free electrons). A large negative voltage is then applied to the target 236, directing the plasma ions 240 to the target 236 and sputtering it, for a period of time, allowing a steady-state to be reached. This time depends on the aspect ratio of the hole and actual dimensions of the hole. For example, a contact hole of aspect ratio 4, with a 0.5 micron opening needs 5 seconds to reach this steady-state. However, a time frame of between approximately 0 to 25 seconds may be required, depending on geometries and setup of the PVD tool.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 11, LINE 10 ENDING ON PAGE 11, LINE 26**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In addition, after a subsequent annealing step, such preferential resputtering further decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to reduce them to titanium oxide and titanium silicide. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce remaining native oxide. In general, between 30 to 50 angstroms of titanium can reduce approximately 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 11, LINE 27 ENDING ON PAGE 12, LINE 6**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

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**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 12, LINE 7 ENDING ON PAGE 12, LINE 19**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

In a second embodiment of the invention, a long-throw PVD apparatus is used to obtain a low grazing angle during resputtering. A Varian M2000 PVD tool, or similar equipment well known to one skilled in the art, is used as shown in Figure 2. However, in this embodiment, the apparatus is noncollimated because a collimator 234 is not used. Instead of using a collimator, a low grazing angle is obtained due to the large substrate-to-target distance. The target 236 power is applied at less than approximately 18 kW. Higher target power provides for a higher deposition rate. The target power is adjusted, so that the desired deposition rate is obtained. A typical argon flow rate is 25 sccm. The target-to-substrate spacing is approximately 450 millimeters. In general, the target-to-substrate spacing is approximately 2 to 3 times greater than that utilized in a collimated setup, and can range from between 100 to 1,000 millimeters, more or less, depending on the relative geometries of the PVD tool and substrate. The target-to-plasma spacing is adjusted, as is well known to one skilled in the art.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 12, LINE 28 ENDING ON PAGE 13, LINE 16**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

After a steady-state is reached, a steady-state resputter scheme is started to redistribute material 150 overhang at the top corner 118 (upper surface) to the bottom corners (on the lower surface) of the contact hole 152, as shown in Figure 1a. The resputtered material 154 on the lower surface 116 of the contact hole 114 has a stoichiometry different than that of the deposited material 150 at the top corner 118, due to the differential resputtering rates of the alloy/composite constituent elements. This resputter scheme is initiated by varying the substrate 110 bias from voltage source 248. For example, using the current setup and contact hole 114 of aspect ratio 4, the zero bias is switched to a small bias (-15 to -65 Volts). In general, the substrate bias voltage should be less than the lowest sputtering threshold energy of any constituent of the alloy target. The amount of material 150 overhang is compensated with the amount of material 154 resputtered, providing a steady state process. The elements in the target material alloy, or composite, resputter at different rates, due to their different atomic masses, resulting in resputtered material being redistributed to the bottom of the contact hole, having a different stoichiometry than the deposited material on the upper surface of the contact hole. In general, heavier elements of a sputtered species sputter at a faster rate than lighter elements. The bias voltage is adjusted according to the elements present in the alloy or composite.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 13, LINE 28 ENDING ON PAGE 14, LINE 15**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

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Serial No.: 09/567,574

In addition, after a subsequent annealing step, such preferential resputtering decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to form titanium oxide and titanium silicide upon subsequent annealing of the material. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $\text{TiSi}_{1.8}$ is adequate to effectively reduce any remaining native oxide. Typically, between 30 to 50 angstroms of titanium can completely reduce 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

| Year | 1990 | 1991 | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036 | 2037 | 2038 | 2039 | 2040 | 2041 | 2042 | 2043 | 2044 | 2045 | 2046 | 2047 | 2048 | 2049 | 2050 | 2051 | 2052 | 2053 | 2054 | 2055 | 2056 | 2057 | 2058 | 2059 | 2060 | 2061 | 2062 | 2063 | 2064 | 2065 | 2066 | 2067 | 2068 | 2069 | 2070 | 2071 | 2072 | 2073 | 2074 | 2075 | 2076 | 2077 | 2078 | 2079 | 2080 | 2081 | 2082 | 2083 | 2084 | 2085 | 2086 | 2087 | 2088 | 2089 | 2090 | 2091 | 2092 | 2093 | 2094 | 2095 | 2096 | 2097 | 2098 | 2099 | 2100 |
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| 1990 | 1991 | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 | 2001 | 2002 | 2003 | 2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 | 2034 | 2035 | 2036 | 2037 | 2038 | 2039 | 2040 | 2041 | 2042 | 2043 | 2044 | 2045 | 2046 | 2047 | 2048 | 2049 | 2050 | 2051 | 2052 | 2053 | 2054 | 2055 | 2056 | 2057 | 2058 | 2059 | 2060 | 2061 | 2062 | 2063 | 2064 | 2065 | 2066 | 2067 | 2068 | 2069 | 2070 | 2071 | 2072 | 2073 | 2074 | 2075 | 2076 | 2077 | 2078 | 2079 | 2080 | 2081 | 2082 | 2083 | 2084 | 2085 | 2086 | 2087 | 2088 | 2089 | 2090 | 2091 | 2092 | 2093 | 2094 | 2095 | 2096 | 2097 | 2098 | 2099 | 2100 | |

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

[illegible]

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The maximum amount of silicon that is consumed from the substrate 310, as shown in Figure 3a, is that needed to form titanium silicide in its equilibrium state. For example, titanium silicide has an equilibrium ratio of silicon to titanium of 2.0:1. When the resputtered material has a ratio of silicon to titanium of less than 2.0:1, silicon is consumed from the substrate to bring the ratio of silicon to titanium back to 2.0:1 after deposition. Compared to prior art techniques, since titanium silicide is being deposited instead of titanium, the profile of the substrate 310 does not change significantly during the process of forming a titanium silicide layer 354 thereon. The resulting layer of titanium silicide 354 provides lower contact resistance due to its generally planar shape. Although the resulting structure has been described in terms of a contact hole 314, deposited with titanium silicide 354, other types of materials and structures can be used, as described previously, without departing from the scope of the invention.

**CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 16, LINE 15 ENDING ON PAGE 16, LINE 22**

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES

Applicant: Frankie Fariborz Roohparvar

Serial No.: 09/567,574

In another embodiment, creating multiple layers of titanium silicides, with a stoichiometry, of TiSi_x , where $x > 2.0$, improves high temperature stability of titanium silicide by approximately 50 to 150 degrees Celsius, depending on how high a value of x device manufacturing processes can tolerate. However, when desired layers of resputtered material comprise a ratio of silicon-to-titanium of greater than 2.0:1, the target material and layer of deposited material must have a ratio of silicon-to-titanium of at least as great as that of the largest ratio of silicon-to-titanium in the resputtered layers of material.

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